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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/924,274	08/07/2001	Paul Metzgen	174/221	4898
36981	7590	02/15/2006	EXAMINER	
FISH & NEAVE IP GROUP			SIEK, VUTHE	
ROPES & GRAY LLP			ART UNIT	
1251 AVENUE OF THE AMERICAS FL C3			PAPER NUMBER	
NEW YORK, NY 10020-1105			2825	

DATE MAILED: 02/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Office Action Summary	Application No. 09/924,274	Applicant(s) METZGEN, PAUL	
	Examiner Vuthe Siek	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 January 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6 and 23-28 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6 and 23-28 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 07 August 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>4/22/03</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is in response to application 09/924,274 and reply filed on 1/17/2005. Election without traverse of Claims 1-6 and cancellation of withdrawn claims 7-22 are acknowledged. Thus claims 1-6 and newly added claims 23-28 remain pending in the application.

Claim Objections

2. Claims 1 and 23 are objected to because of the following informalities: phrase "possible optimizations" should be changed to --optimizations-- in order avoid uncertainty in the claim language; "a more efficient implementation" needed clarification because the phrase appeared to be a relative term which is must be clarified in what area; and "a program" and "software constructs" also needed to be specific as to what they are. In addition, in "where using software constructs comprises establishing communications between the programmable logic circuit and at least one software device", what one software device is referred to and is it different from software constructs, how using software constructs would establish communications between the programmable logic circuit and at least one software device. Appropriate correction is required. Note that Examiner has rejected claims based reasonably interpretation of the claim language.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11

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F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1-6 and 23-28 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 20-26 of copending Application No. 09/924,272. Although the conflicting claims are not identical, they are not patentably distinct from each other because the instant application and the copending application claim the same subject matter of optimizing a circuit, where an optimized circuit is generated using a software-to-hardware compiler at a later stage of the compilation. Although, the copending application does not disclose analyzing a circuit, it would be obvious to practitioners of the art because the analyzing circuit would have been used as part of optimization of the circuit in order to effectively generate the optimized circuit as implemented.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

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A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-6 and 23-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Agarwal et al. (5,761,484).

7. As to claims 1 and 23, Agarwal et al. teach a compilation technique to overcome device pin limitations using virtual interconnections. The virtual interconnections are established by software or hardware compiler programs between programmable logic devices (col. 2 lines 36-51). A virtual interconnection represents a connection from logical output one programmable logic device to a logical input of another programmable logic device. The resulting improvement in bandwidth reduced the need for global routing allowing effective use of low dimension inter-chip connections (such as nearest-neighbor). The software compiler utilizes static routing or dynamic routing and relies on minimum hardware support (col. 2 lines 1-67, col. 12 lines 1-15). The establishment of virtual interconnections corresponds to establishment of communications between the programmable logic circuit and a least one software device. Agarwal et al. suggest the method of optimizing the circuit using virtual interconnections between programmable logic devices provides mapping efficiency (col. 9 lines 61-67) and using timing and/or locality sensitive partitioning with virtual interconnections has potential for reducing the required number routing sub-cycles. The communication bandwidth can be further increased with pipeline compaction, a technique of overlapping the start and end of long virtual path with shorter paths traveling in the same direction. A more robust implementation of virtual interconnections

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replaces the global barrier imposed by routing phases with a finer granularity of communication scheduling, possible overlapping computation and communication as well (col. 11 lines 55-67, col. 12 lines 1-6). Note that logical inputs and logical outputs corresponding to software constructs are used to establish virtual interconnections (communications) as claimed (Fig. 3).

8. As to claim 2 and 24, Agarwal et al. teach using software-to-hardware compiler to analyze the circuit at a later stage in a compilation (col. 2 lines 65-67).

9. As to claim 3 and 25, Agarwal et al. teach analyzing the circuit's critical path (col. 2 lines 65-67, col. 7 lines 31-50).

10. As to claim 4-5 and 26-27, Agarwal et al. teach placing at least one register and at least one FIFO in the circuit (col. 7 lines 30-37; col. 7 lines 58-67; col. 8 lines 1-46; col. 9 lines 1-23; Figs. 3, 6).

11. As to claim 5 and 27, Agarwal et al. teach placing at least one interface buffer in the circuit (Fig. 7).


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek


VUTHE SIEK
PRIMARY EXAMINER